High Voltage Current Buffer

INTRODUCTION

Many high voltage op amps cannot deliver more than 200mA of output current. For applications requiring as much as 1A of current, you can include the current buffer described here. The current buffer is designed to provide approximately unity voltage gain and is inserted between the output of the high voltage op amp and the load. The current buffer is included in the feedback loop of the operational amplifier and creating a composite op amp.

One of the design challenges with a current buffer is the output stage bias circuit. A Class B output stage may be adequate for some applications, but it has characteristic crossover distortion as the lower device output current transitions to the high side device. A Class AB output stage is usually preferred as the crossover distortion is much lower and the feedback loop remains closed during the transition. Setting the quiescent current of the Class AB output stage is difficult because of output device variations and sensitivities.

The current buffer design approach proposed here avoids many of the difficulties of output stage biasing by incorporating a depletion mode MOSFET as the high side driver. This circuit topology exploits the MOSFET's ability to be used as a current source to provide the bias current. The depletion mode MOSFET serves as the bias current generator as well as the high side driver.

TYPICAL CURRENT BUFFER TOPOLOGIES

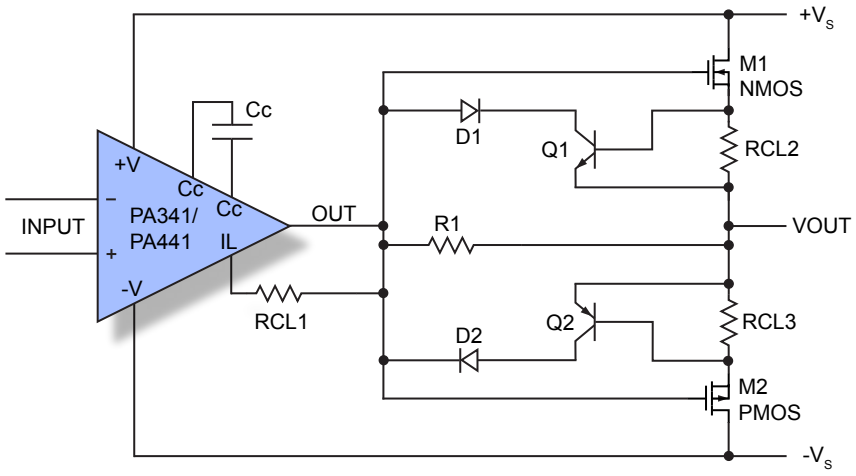

Figure 1: Class B Current Buffer

The Class B circuit shown in Figure 1 illustrates one common method of implementing a current buffer. The resistor R1 provides a current path to the load from the op amp and is selected to limit the maximum gate voltage of M1 and M2 to 10V. The resistor RCL1 sets the current limit value of the PA341 so that the current in R1 creates a voltage drop of 10 Volts. The op amp current limit value should be set as low as possible to minimize power dissipation of the op amp. Resistors RCL2 and RCL3 are included as a method of current limiting the output MOSFETs M1 and M2. This provides a level of protection for the output devices.

The output current flows through RCL2 and RCL3 creating a voltage across the base to the emitter of Q1 and Q2. Once this voltage reaches approximately 0.7V, the transistors Q1 and Q2 begin conducting current to the load thus clamping the gate drive voltage at M1 and M2 as the PA341 enters current limit mode.

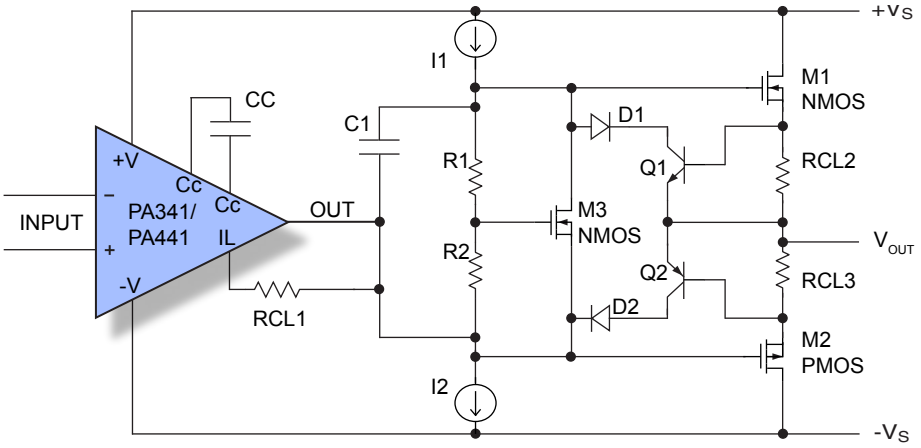

Figure 2: Conventional Class AB Current Buffer

Figure 2 is a simplified schematic diagram of the conventional circuit topology used for a Class AB output stage. The VGS multiplier composed of M3, R1 and R2 sets the required voltage at the gates of M1 and M2 which provides the desired quiescent current through the output devices, M1 and M2. Constant current sources I1 and I2 provide the required current to the VGS multiplier. The transistors Q1 and Q2 are used for current limiting as described in the previous example of the Class B stage.

This design approach is much more complex and problematic than the Class B stage design. The current sources I1 and I2 require additional components in the actual implementation. The voltage swing will be less than the voltage swing of the PA341 because of the drive requirements of the output MOSFETs. Setting the quiescent current through M1 and M2 is difficult because of the high sensitivity between VGS and ID. The VGS multiplier, consisting of M3, R1 and R2 must be individually adjusted for every unit. Preventing thermal runaway relies on device matching and tight thermal coupling between M1, M2 and M3. Thermal stability is difficult to achieve. Because of the circuit complexity, temperature instability and sensitivity in setting the quiescent current, the actual implementation of this circuit topology is much more challenging than that of the Class B version

ALTERNATE CLASS AB CIRCUIT DESCRIPTION

A conceptual simplified circuit diagram of the proposed topology is shown in Figure 3. To demonstrate the mechanism for establishing the flow of quiescent current, assume the output voltage is at zero V. The base of Q1 must be approximately -0.7V. The Gate of M1 is also at -0.7V forcing the MOSFET to conduct. The resistor RS, is selected to adjust the quiescent current to the desired value. This circuit functions in a self-biasing mode and does not require the current sources and Vgs multiplier of the conventional Class AB stage.

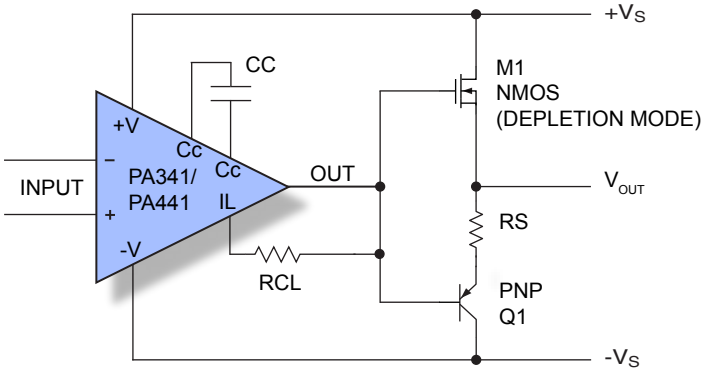

Figure 3 Alternative Class AB Current Buffer

The actual prototype circuit schematic is shown in Figure 4. The depletion mode MOSFET M1, is biased to provide the quiescent current for the output stage. The resistors R4 and R5 are selected to establish the operating current of M1. The bipolar transistor Q1, acts as a Vbe multiplier maintaining the desired Vgs for M1 as demand for load current increases. So Q1 essentially conducts the output current sourced by M1 by bypassing R4 and R5. The bipolar transistors Q2 and Q3, are biased by the quiescent current and provide the load current during the negative half cycle. Two PNP transistors were necessary to accommodate the required power dissipation. The maximum rated power dissipation of each PNP transistor is 50W. The current limit function is implemented through the addition of diodes D1 through D6. The diodes used in the prototype are 1N4148, but any equivalent small signal switching diode such as 1N914 is suitable. When the output current approaches approximately 1.2A, the voltage across R6 in series with the Vbe of Q1 forces Q1 to limit the output current. Since the diodes D1 and D2 are conducting, a constant current through Q1 is established. The maximum output current delivered by the PA341 is set to approximately 40mA by Rcl. The diodes D5 and D6 clamp the output of the PA341 to limit the Vgs of M1 and still provide sufficient gate drive voltage to support the load current. When the current limit function is engaged, the output current of the PA341 flows through D1, D2, D5 and D6. The current limit for the negative half cycle functions by forcing output current from the PA341 through diodes D3 and D4, which establishes a constant current of approximately 1.2A through Q2 and Q3.

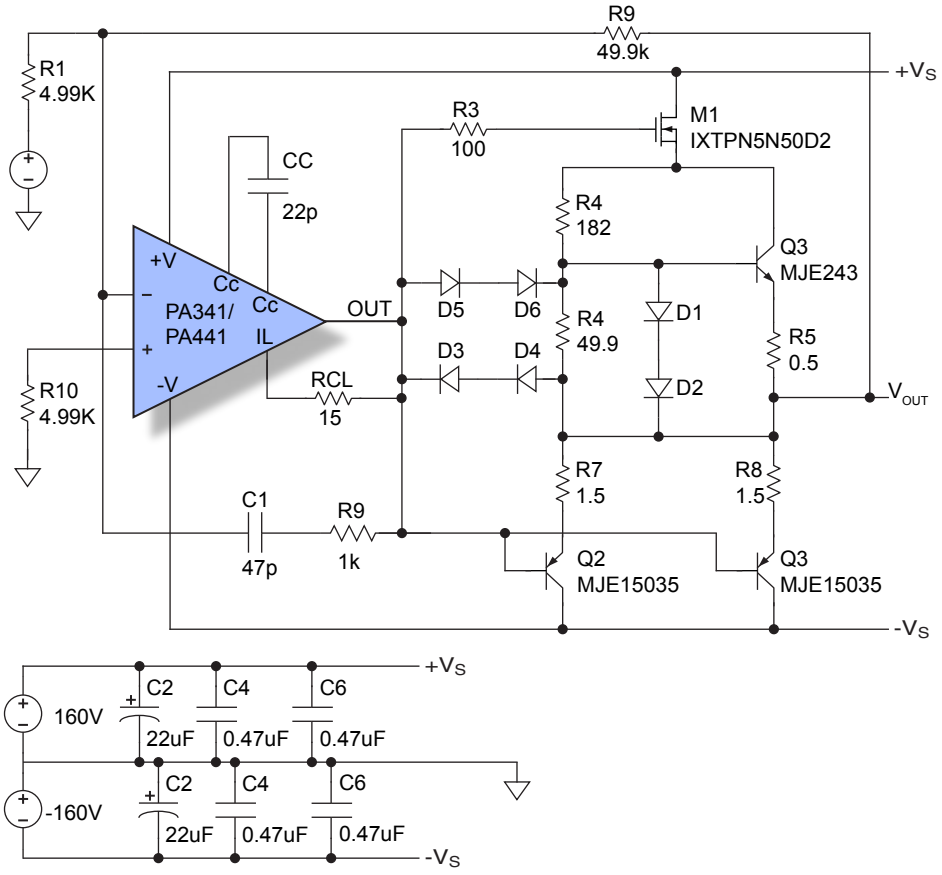

Figure 4: Schematic Diagram of Class AB Current Buffer as Assembled and Tested

The advantages of this topology are:

1. High output voltage swing because of limited voltage drop as compared to the typical enhancement mode Class AB output stage.
2. Simplicity of setting quiescent current
3. Reduced component count

The simulation plots of Figure 5 illustrate circuit operation under light load conditions. The output voltage is 100V p-p across a load resistor of approximately 7KΩ. The plots indicate a quiescent current of approximately 9mA. Since the current through the transistors, M1, Q2 and Q3 is always greater than zero for the entire cycle, the output stage is operating in Class A mode.

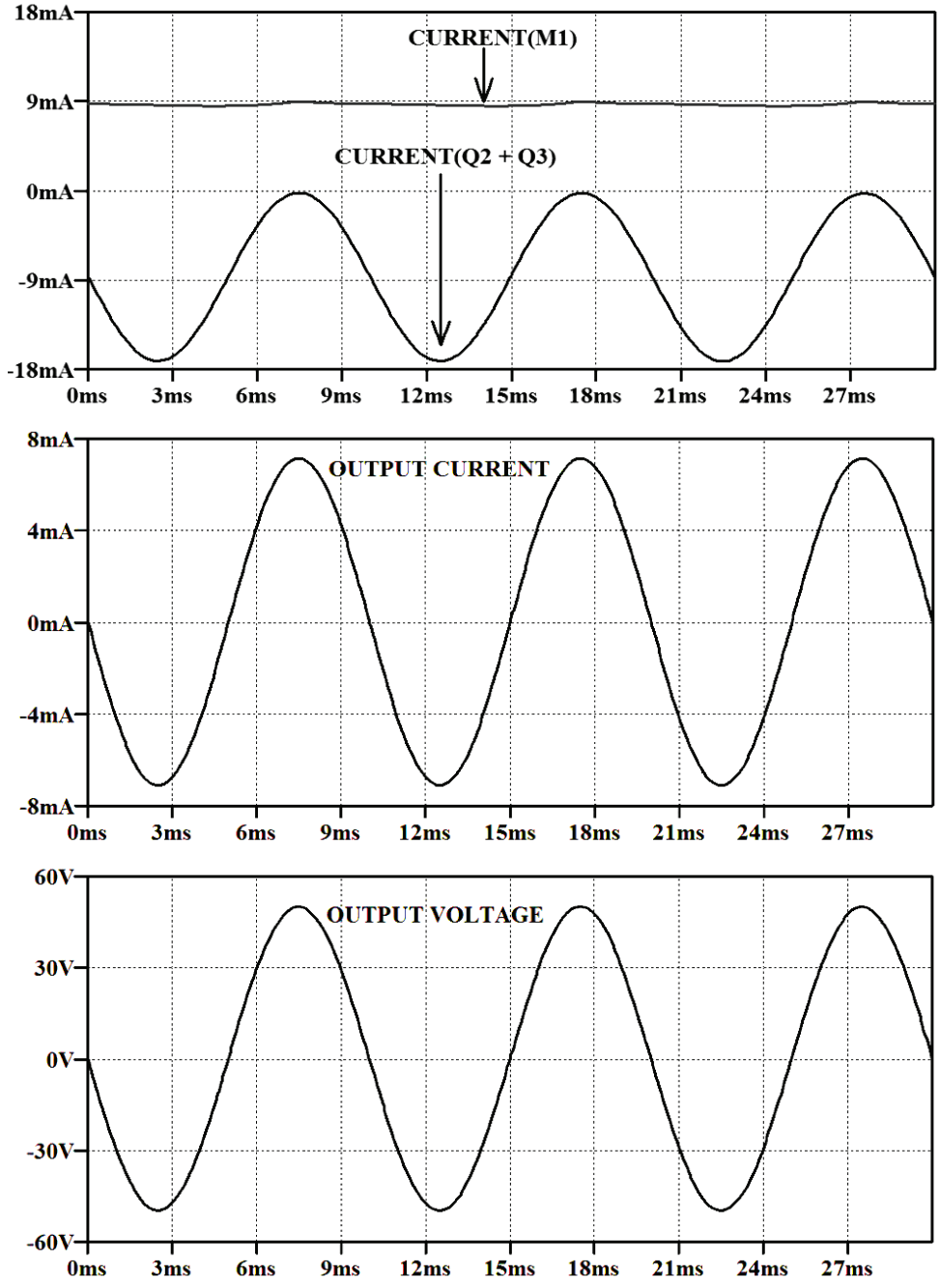

Figure 5: Output Stage Behavior in Class A Mode (light load)

The simulation plots of Figure 6 Illustrate circuit operation under full load conditions. The power supply voltage is ±160V. The output voltage is 200V p-p across a load resistor of 100Ω. The output stage is operating in Class AB mode.

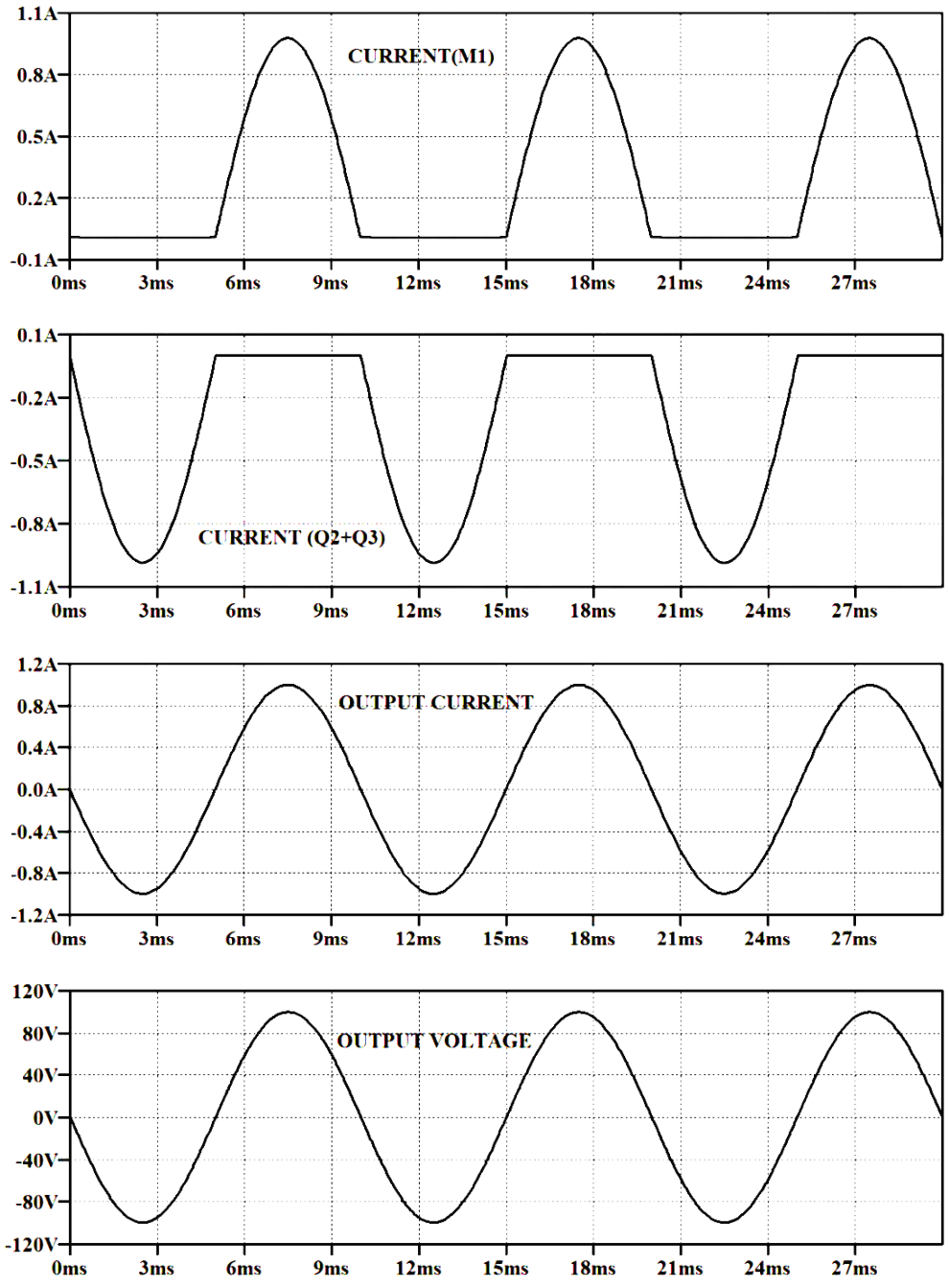

Figure 6: Output Stage Behavior in Class AB Mode (full load)

Figures 7, 8, 9 and 10 are oscilloscope screen shots taken during bench testing showing the actual circuit behavior. Power supply voltage is ±160V, signal frequency is 10KHz with the amplifier configured for an inverting gain of 10. The actual circuit configuration is shown in Figure 4. Channel one is the output voltage and channel two is the input voltage.

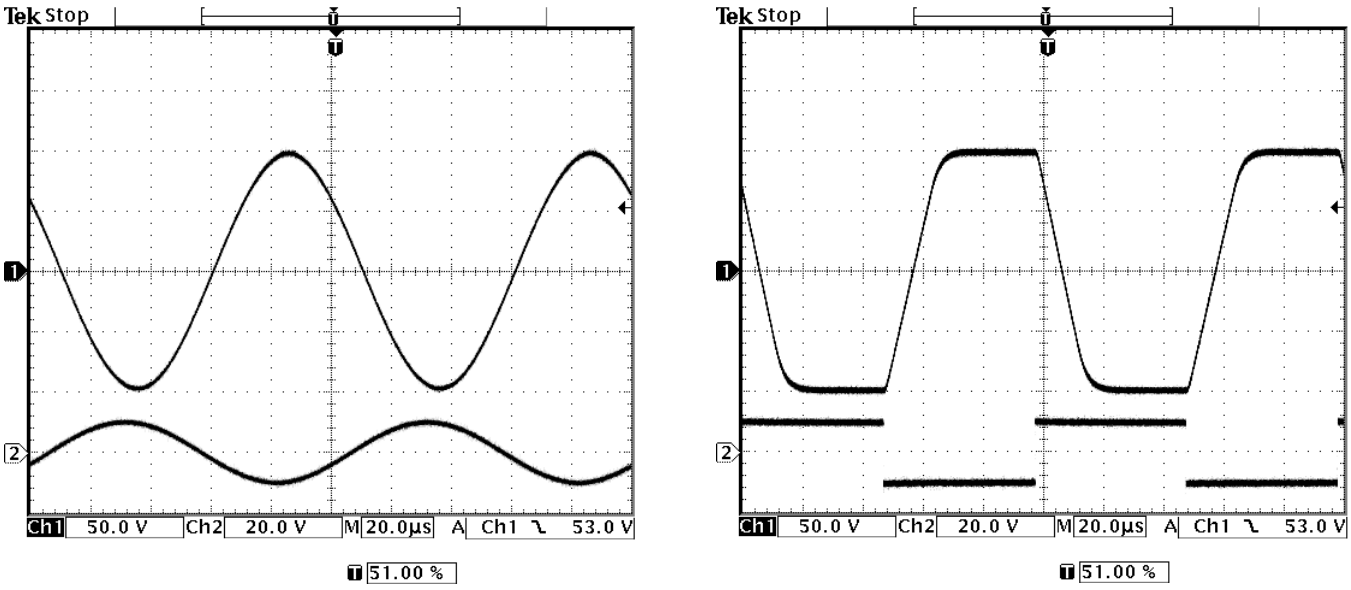

Figure 7: Oscilloscope Waveforms of Output voltage with Capacitive load of 0.1µF in Series with 10Ω

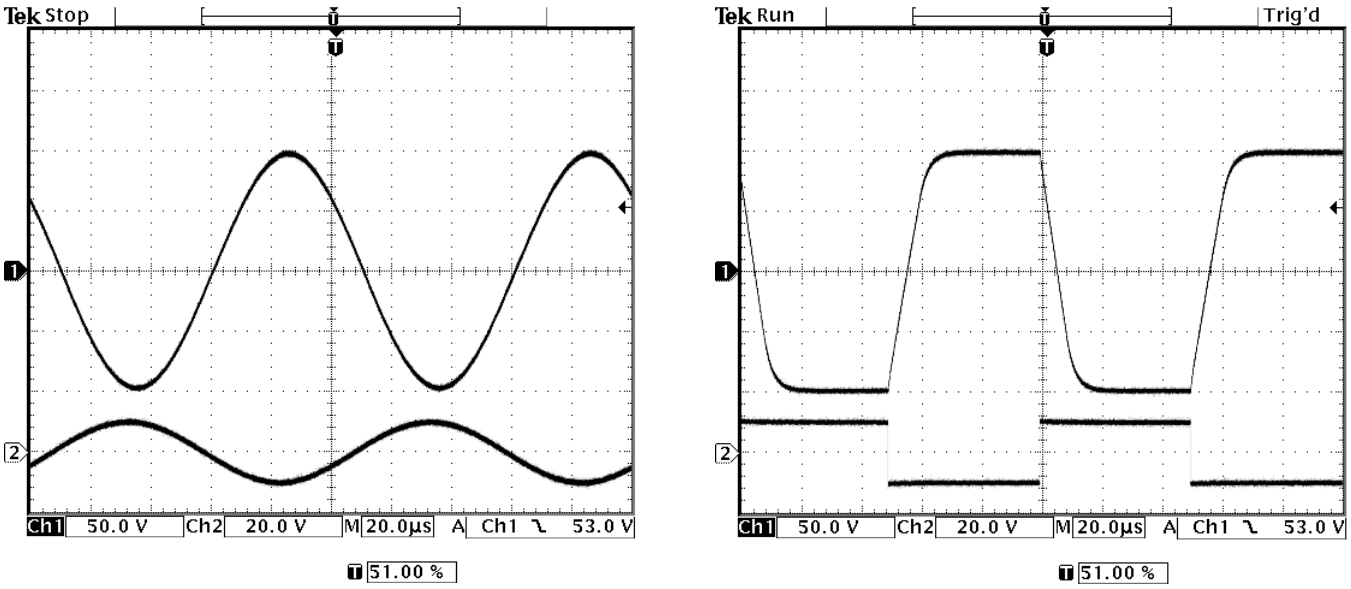

Figure 8: Oscilloscope Waveforms of Output Voltage with Resistive Load of 100Ω

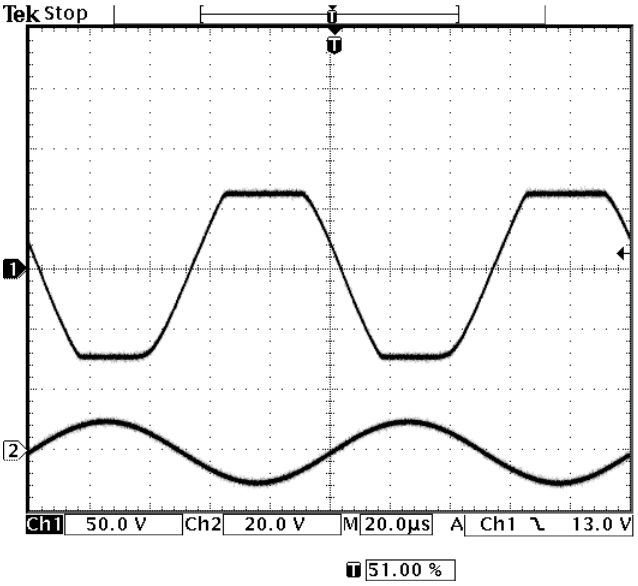

Figure 9: Oscilloscope Waveform of Output Voltage Showing Current Limit Levels with Resistive load of 50Ω

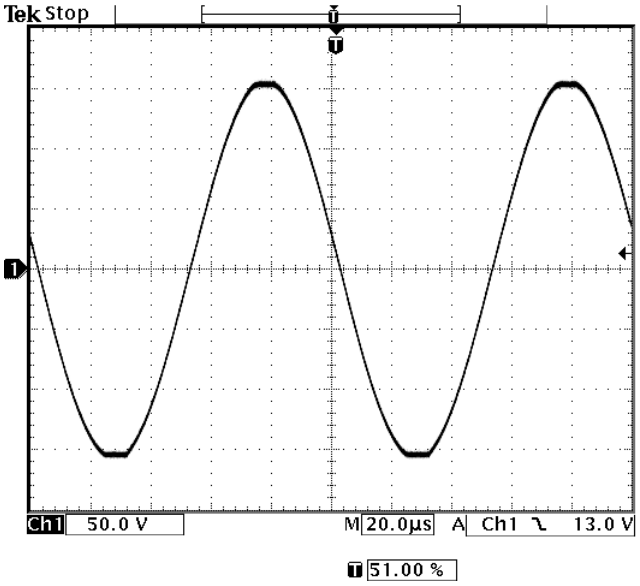

Figure 10: Oscilloscope Waveform of Output Voltage Showing Voltage Swing Clipping. Power Supply Voltage is ±160V with Resistive Load of 150Ω (1AMP)

REFERENCES

1.Graeme, Tobey, Huelsman; OPERATIONAL AMPLIFIERS Design and Applications, 1971, McGraw-Hill
2.Steele, Eddlemon; Use High-Voltage Op Amps to Drive Power MOSFETs, Electronic Design, June 24, 1993
3.PA341U, Data Sheet, High Voltage Power Operational Amplifier, Apex Microtechnology: www.apexanalog.com
4.PA441U, Data Sheet, High Voltage Power Operational Amplifier, Apex Microtechnology: www.apexanalog.com